SERIAL LINE INPUT/OUTPUT SYSTEM

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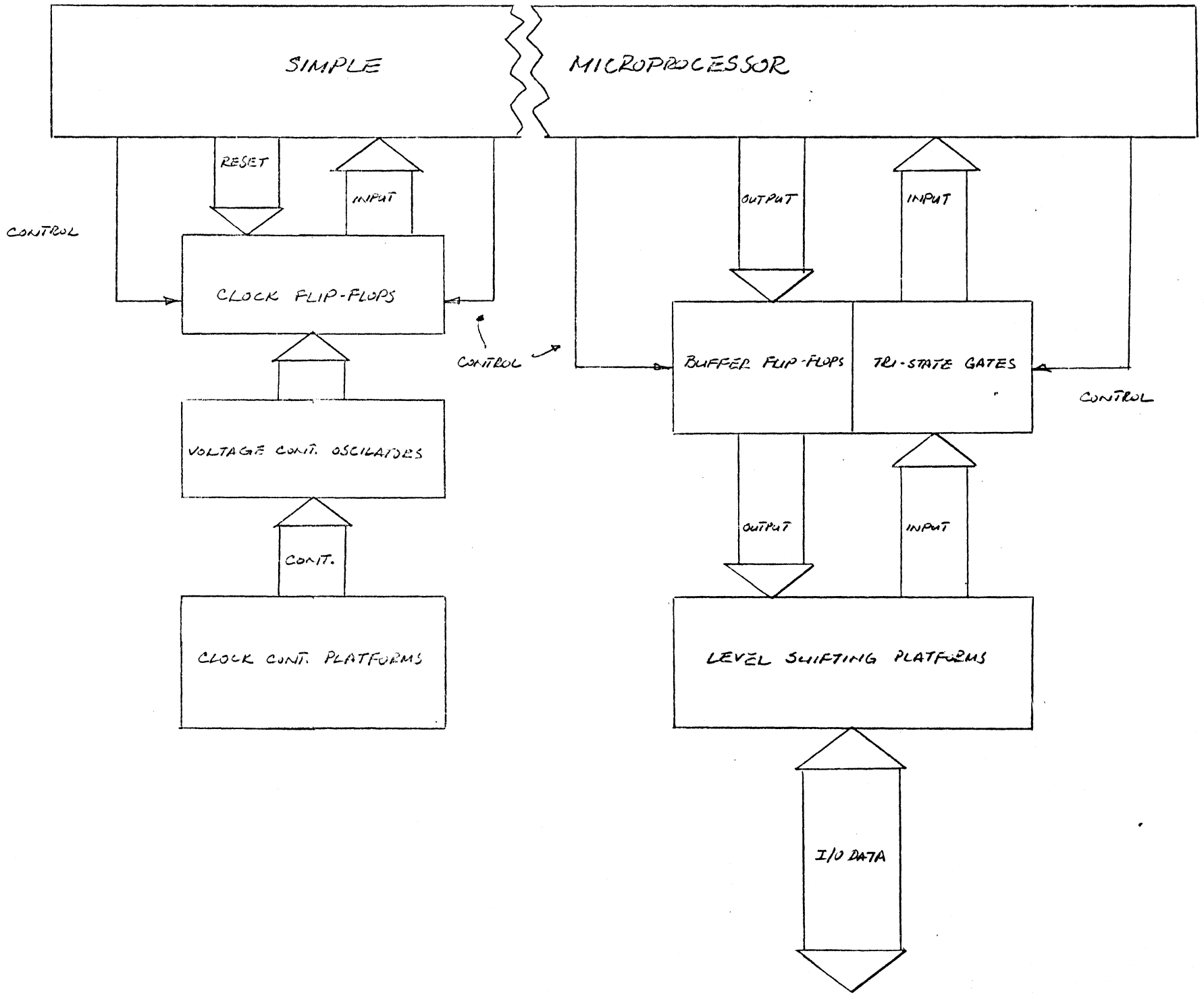
Introduction

The serial line input/output system for the C.R.M.S. interactive computer is constructed from a combination of hardware, microcode, and software. The system interfaces with up to 64 serial I/O devices and can accommodate up to eight different data rates simultaneously. New I/O devices with perhaps different data rates may be easily added or substutited.

The Hardware Interface

From the point of view of the SIMPLE microprocessor the hardware interface consists of ten different I/O devices: four 16 bit wide input devices, four 16 bit wide output devices, one 8 bit wide clock input device, and one 8 bit wide clock reset output device. Also, the logical "OR" of all eight of the clocks is constantly available to the SIMPLE microprocessor. This attention line is raised whenever any of the eight clocks are set and acts as an alert of an I/O servicing need. Each of the four input devices consists of 16 tri-state gates which, when enabled, transfer data from the 16 I/O lines into the SIMPLE microprocessor's I/O register. Each of the four output devices consists of 16 buffer flip-flops which, when clocked, buffer data from the SIMPLE microprocessor's I/O register and make this data available to the 16 I/O lines. Common to the gates and buffer flip-flops is 16 electrical interface plug-in platforms which provide for level shifting of I/O signals. The 8 bit wide clock input device consists of eight voltage controlled oscilators, eight plug-in clock platforms, and eight buffer flip-flops which are shared with the clock reset device. A clock platform consists of a capacitor which sets the center frequency of the oscilator and an adjustable resistor which trims this center frequency. The buffer flip-flops are set by a positive voltage swing of the oscilators and, when selected are reset by the SIMPLE microprocessor from its I/O register.

When an I/O device is connected to any of the 64 I/O lines one of the oscilators is adjusted to match the data rate of the device. Whenever this clock comes up the SIMPLE microprocessor initiates a Multiplexer microcode routine to service the device and, as determined by software, picks up an input data bit and/or gates an output data bit to the device.



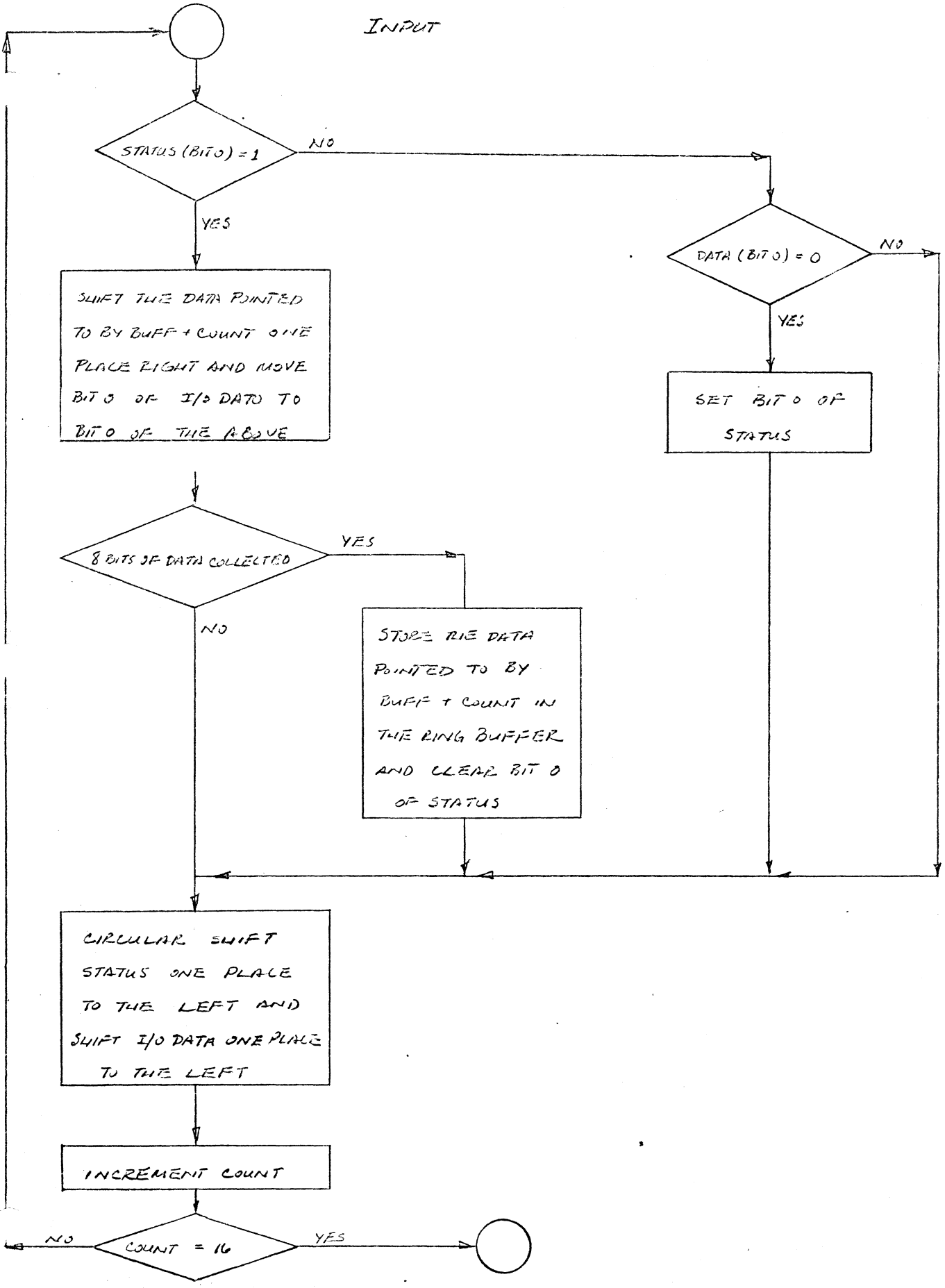
FUNCTIONAL LAYOUT OF THE
SERIAL LINE HARDWARE INTERFACE

The Serial line Multiplexer

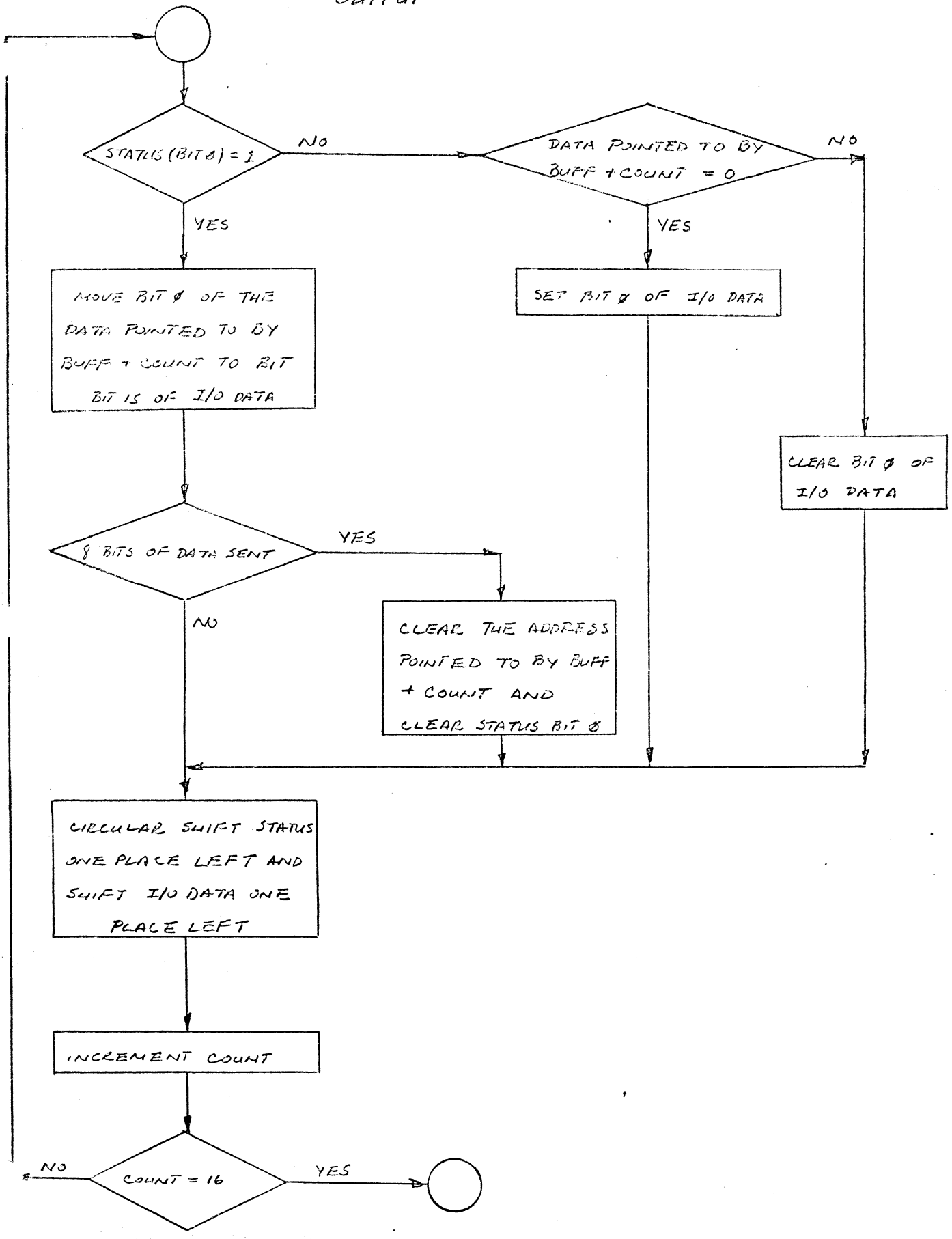
The serial line multiplexer is the name of a microcode functional unit of the SIMPLE microprocessor of the C.R.M.S. interactive computer.

Associated with each group of 16 I/O lines there is a storage buffer area in core which holds 16 words of partially assembled input data, 16 words of partially dissembled output data, 2 16 bit status words, and a hardware device address word. If in the input status word bits 1, 5, and 12 are set while all the rest are off this indicates that of the 16 lines associated with the portion of the hardware interface determined by the contents of the hardware device address word the only lines that are in the process of transfering a string of input data are lines 1, 5, and 12 while all the others are in an inactive state. A similar situation prevails for the output status word.

Whenever any of the serial line clocks sets its buffer flip-flop, the SIMPLE microprocessor transfers control to the Multiplexer. The multiplexer then determines which of the four groups of 16 I/O lines needs attention, resets the appropiate clock(s), sets a pointer called BUFF to the proper storage buffer described above, sets a counter called COUNT to zero and then transfers control to its multiplexining input and/or output subroutine. A slightly simplified flow chart of these two routines is presented on the following pages.


INPUT
STATUS (BIT 0) = 1
NO
YES
DATA (BIT 0) = 0
NO
YES
SHIFT THE DATA POINTED TO BY BUFF + COUNT ONE PLACE RIGHT AND MOVE BIT 0 OF I/O DATA TO BIT 0 OF THE ABOVE
SET BIT 0 OF STATUS
8 BITS OF DATA COLLECTED
YES
NO
STORE RIE DATA POINTED TO BY BUFF + COUNT IN THE RING BUFFER AND CLEAR BIT 0 OF STATUS
CIRCULAR SHIFT STATUS ONE PLACE TO THE LEFT AND SHIFT I/O DATA ONE PLACE TO THE LEFT
INCREMENT COUNT
NO
COUNT = 16
YES

OUTPUT


STATUS (BIT 0) = 1
NO
DATA POINTED TO BY BUFF + COUNT = 0
NO
YES
YES
MOVE BIT 0 OF THE DATA POINTED TO BY BUFF + COUNT TO BIT BIT IS OF I/O DATA
SET BIT 0 OF I/O DATA
CLEAR BIT 0 OF I/O DATA
8 BITS OF DATA SENT
YES
NO
CLEAR THE ADDRESS POINTED TO BY BUFF + COUNT AND CLEAR STATUS BIT 0
CIRCULAR SHIFT STATUS ONE PLACE LEFT AND SHIFT I/O DATA ONE PLACE LEFT
INCREMENT COUNT
NO
COUNT = 16
YES

The destination of assembled input data and the source of assembled output data to be multiplexed by the input/output microcode routines is a ring buffer. This ring buffer is the interface between the multiplexer and a software process which handles serial device interactions.

Summary

The initial system has been set up to interface with 64 teletypes but it should be emphasized that the I/O system is not limited to teletypes. In fact, with appropiate changes in microcode, the system may communicate with any mix of serial and parallel I/O devices; the only limitation being that the total number of lines used cannot exceed 64 and the total number of different data rates cannot exceed 8. By changing a plug-in electrical level shifting platform an electrically different I/O device may be added or substutited easily and economically while logically different I/O devices are accomodated by changes in microcode. From a hardware point of view the Serial line I/O system is extremely economical to construct and as an additional benifit, the hardware may be easily debugged, in the event of a failure on the circuit borad, by the systems programmer at the machine's programmer's panel.